AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) Apparatus for processing data operable to execute operations specified in a stream of program instructions, said apparatus comprising:

(i) a hardware based instruction execution unit operable to execute program instructions; and

(ii) a software based instruction execution unit operable to execute program instructions; wherein

(iii) program instructions to be executed are sent to said hardware based execution unit for execution;

(iv) program instructions received by said hardware based execution unit for which execution is not supported by said hardware based execution unit are forwarded to said software based execution unit for execution with control being returned to said hardware based execution unit for a next program instruction to be executed; and

(v) said hardware based execution unit includes scheduling support logic operable to generate a scheduling signal for triggering a scheduling operation to be performed between program instructions for managing scheduling between threads or tasks irrespective of whether a preceding program instruction was executed by said hardware based execution unit or said software based execution unit.

2. (Original) Apparatus as claimed in claim 1, wherein said scheduling support logic includes a counter with a value that is changed in response to a program instruction sent to said hardware based execution unit.

3. (Original) Apparatus as claimed in claim 2, wherein said counter triggers generation of said scheduling signal when a predetermined count value is reached.

4. (Original) Apparatus as claimed in claim 3, wherein said counter may be programmed to start from a user programmable start value.

5. (Original) Apparatus as claimed in claim 3, wherein said counter counts up to said predetermined value.

6. (Original) Apparatus as claimed in claim 3, wherein said counter counts down to said predetermined value.

7. (Original) Apparatus as claimed in claim 1, wherein a debug operation is triggered by said scheduling signal.

8. (Original) Apparatus as claimed in claim 1, further comprising timer logic operable to generate a timer signal indicative of a time since a last scheduling operation.

9. (Original) Apparatus as claimed in claim 8, wherein said scheduling signal is combined with said timer signal to trigger said scheduling operation.

10. (Original) Apparatus as claimed in claim 8, wherein a scheduling operation is triggered upon generation of said scheduling signal after said timer signal has reached a predetermined value indicating a predetermined period time since a last scheduling operation has expired.

11. (Original) Apparatus as claimed in claim 1, further comprising a processor core operable to execute operations as specified by instructions of a first instruction set.

12. (Original) Apparatus as claimed in claim 11, where said hardware based instruction execution unit includes an instruction translator operable to translate instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set.

13. (Original) Apparatus as claimed in claim 12, wherein

(i) at least one instruction of said second instruction set specifies a multi-step operation that requires a plurality of operations that may be specified by instructions of said first instruction set in order to be performed by said processor core; and

(ii) said instruction translator is operable to generate a sequence of translator output signals to control said processor core to perform said multi-step operation.

14. (Original) Apparatus as claimed in claim 1, wherein said software based execution unit is a software based interpreter.

15. (Original) Apparatus as claimed in claim 1, wherein said program instructions are Java Virtual Machine instructions.

16. (Currently Amended) A method of processing data by executing operations specified in a stream of program instructions, said method comprising the steps of:

(i) executing program instructions with a hardware based instruction execution unit; and

(ii) executing program instructions with a software based instruction execution unit; wherein

(iii) program instructions to be executed are sent to said hardware based execution unit for execution;

(iv) program instructions received by said hardware based execution unit for which execution is not supported by said hardware based execution unit are forwarded to said software based execution unit for execution with control being returned to said hardware based execution unit for a next program instruction to be executed; and

(v) said hardware based execution unit generates a scheduling signal for triggering a scheduling operation to be performed between program instructions for

managing scheduling between threads or tasks irrespective of whether a preceding program instruction was executed by said hardware based execution unit or said software based execution unit.